AN ANALYSIS OF NOVEL 12T SRAM CELL WITH IMPROVED READ STABILITY

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ABSTRACT- Improvement of nanotechnology increases demand of scaling in CMOS technology. Stability is a main future concert for memory cell to avoid data loss. In this paper, a novel 12T SRAM cell is proposed which used Schmitt trigger circuit to increase stability and a transistor to reduce leakage current in standby mode. The read stability is major aspect which is measured and compared in this paper. The stability of read operation and ability of write operation are measured by using N-curve method using 32 nm technologies and simulated under spice simulator tool. The read stability in proposed cell is found to be better 1.1X and same as compare to the 6T and 8T SRAM Cell respectively.

KEYWORDS- SRAM Cell, Stability, N-curve method, Schmitt trigger, leakage current.

1. INTRODUCTION

Stability is the main concern of semiconductor memories. SRAM cell are widely used in semiconductor devices and these days, semiconductor devices need to enhance nanotechnology scaling in CMOS (Complementary metal–oxide–semiconductor) to make enhanced performance in SRAM cell. Nanotechnology scaling affects stability in SRAM cell directly. Stability depends on maximum noise that can be tolerated by memory cell and scaling in memory cell will increase noise and data loss. Various methods and technologies were introduced to improve the write margin and read stability of SRAM Cell. Mobile devices are essential part of our day to day life and to make it more reliable we required more stability in scaling at low power supply. Mobile devices mainly required low power and more stable SRAM cell to fulfil new requirements. To enhance stability normally we use static noise margin (SNM) curve. But still static current noise margin (SINM) has to be derived by mathematical calculation of the measured...
data in SNM curve [1]. We apply N-curve in this paper which measure SINM, WTI, SVNM, and WVT. Different designs of SRAM cell with 6 to 10 transistors have been proposed by researcher which is measured by using N-curve. Thus, as described in (S. Pal et al.) 2016. [2]

We have discussed on our new proposed cell and comparing it with 6T and 8T SRAM cell. The limitations present in conventional 6T SRAM cell which is improved in our new cell. Our main purpose is to improving stability by avoiding data flipping problem which is associated with conventional 6T SRAM cell [3]. So, in our proposed cell we use separate read and write port to make cell more stable. We use Schmitt trigger circuit to improve stability and avoid data flipping through internal node of cell. Another technique we apply in this paper to reduce leakage current by using Conventional transistor in our proposed 12T SRAM cell to optimise N-curve [4].

2. PROPOSED CELL

This paper proposed novel 12T SRAM architecture to achieve high stability. The proposed design is read/write decoupled circuit with one Schmitt trigger and one Conventional transistor. The proposed cell perform read and write operation separately. Separate operations help to increase stability in SRAM cell. Schmitt trigger are connected to the node of the Q and bit line bar. Conventional transistor connected to source of M11 and M3, which is used to enhance stability as shown in Fig. 1.

The Schmitt trigger is used to provide feedback mechanism to input transistor in SRAM cell to reduce the limitation of read and write access time. When Schmitt trigger improved the mechanise of input of the cell then, Data will be stored in cell for a longer time and it will be automatically improve the stability in read and write operation[5].

The Conventional transistor introduced in both inverters is used to reduce leakage current and enhance stability [6]. Conventional transistor was also helping to robust the sub-threshold leakage current in SRAM cell. Additionally, Conventional transistor helps to control leakage current due to stacking effect. The sub-threshold leakage is an important factor which is reduced by stacking effect in hold mode condition [7][8].
2.1 WRITE OPERATION

During write operation of the proposed SRAM cell, write signal is high while read signal is maintained low. We kept voltage constant equal to $V_{dd}/2$. If we want to write 0, then we assume that bit line bar equal to $V_{dd}$ and bit line equal to 0. Initially, both access transistors are turned high. Access transistor M5 is forcedly pull down QB Node [9] and then M4 is tuned as shown in Fig 2(a). Now new value can be written which make bit line equal to 0 and bit line bar equal to $V_{dd}$ [10]. Schmitt trigger is used between M3 and M7 and it will give frequently triggering to increase speed of storing data.
2.2 READ OPERATION

During read operation, Read signal is maintained high while write signal is maintained low. The read access transistor M7 is activated. When Q stores “1”, BL is discharged through M5 and M7. Alternatively, when QB stores “1”, the complementary bit line (BLB) is discharged through M6 and M7. Since M3 and M4 are disconnect completely, during read operation storage node Q and QB are completely isolated as shown in Fig. 2(b). Isolation of storage node helps to increase stability compare to a conventional 6T SRAM cell which is shown below in the results of comparative table. In this paper we measure stability in read operation through N-curve method [11].

3. METHODOLOGY

To evaluate stability in SRAM cell, we simulated these cells through N-curve and measure SVNM, SINM, WTV, WTI. These parameters measure the stability of read / write operation [12]. To measure N-curve, we clamped both bit lines at Vdd and word line is high for read condition.[13]. Different topologies of SRAM cell compared and evaluated in N-curve by measuring SVNM, SINM, WTI and WTV. To get improved read stability, SPNM (Mean of SVNM and SINM) should be higher in value. To get improved write stability, WTP (Mean of WTV and WTI)[14] should be lower in value.[15]

3.1 The static voltage noise margin (SVNM)
The static voltage noise margin is the voltage difference between two points a and b as shown in fig. 4 and SVNM shows the maximum tolerable noise at the input of the storage node in the cell before its content flip as shown in Fig. 3.

3.2 The static current noise margin (SINM)

The static current noise margin is defined as the highest value of current that can be injected in the cell before its content changes. It is given by the peak value of current in read operation to be precise between two points a and b.

3.3 THE WRITE–TRIP VOLTAGE (WTV)

The write–trip voltage shows the minimum voltage drop essential to flip the internal nodes of the cell with both the bit lines clamped at Vdd. WTV is the voltage difference between two points c and b which can be help to measure write stability as shown in Fig. 3.

3.4 THE WRITE TRIP CURRENT (WTI)

Write Trip Current is the amount of minimum current needed to write the cell when both bit lines are clamped at supply voltage equal to Vdd. It is given by the peak value of current in write operation to be precise between two points c and b [14].

Fig 3.N-curve of Read Stability in a Proposed 12T SRAM Cell

4. EXPERIMENTAL RESULTS (CELL READ STABILITY ANALYSIS)

In this paper, we have considered N-curve cases of SRAM configurations and compare them. The stability is significant parameter for SRAM cell [16]. Hence we compare the stability of proposed SRAM cell with 6T and 8T SRAM cell stability as shown in Table 1. We have two commonly used techniques to analysis stability in
SRAM cell. Static noise margin (SNM) and N-curve are generally used methods to calculate stability in SRAM cell. SNM curve is most common technique to measure stability in SRAM cell from earlier time. But lack of inline tester is a drawback of SNM technique [17]. Another drawback of SNM is the limitation of voltage scaling below $V_{dd}/2$ [15]. The N-curve method easily measure inline tester measurement in SINM and easily measure below $V_{dd}/2$ as shown in Table 2. In N-curve method we calculate overall stability through both current and voltage as SVNM and SINM which is not happen in SNM method.

<table>
<thead>
<tr>
<th>TABLE I. SRAM CELL STABILITY</th>
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<tbody>
<tr>
<td>CELL</td>
</tr>
<tr>
<td>SINM[µA]</td>
</tr>
<tr>
<td>SVNM[mV]</td>
</tr>
<tr>
<td>WTI[µA]</td>
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<tr>
<td>WTV[mV]</td>
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Table 2. Comparative table of SPNM and WPI of SRAM cell

<table>
<thead>
<tr>
<th>CELL</th>
<th>Conventional 6T SRAM Cell</th>
<th>8T SRAM Cell [18]</th>
<th>Proposed 12T SRAM Cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPNM</td>
<td>183.59</td>
<td>201.53</td>
<td>202.055</td>
</tr>
<tr>
<td>WPI</td>
<td>343.015</td>
<td>312.45</td>
<td>322.205</td>
</tr>
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5. CONCLUSION

This work proposed a noble 12T SRAM cell which is suitable for high stability. In this paper, we introduced N-curve method for analysing read stability of the SRAM cell. We improved read stability through the N-curve metrics in the proposed 12T SRAM cell and compared it through other cells. Proposed 12T SRAM cell operates at 25°C at 1volt power supply. Simulation results shows that, the proposed 12T SRAM cell gives high read stability with similar power supply voltage and temperature compares to conventional 6T SRAM and other cells.
REFERENCES


